

WHAT IS CLAIMED IS:

- 1 1. Anelastic store circuit which absorbs a propagation delay
2 time difference among plural pieces of data, comprising:
3 a clock selector for selecting a read clock from a
4 plurality of clocks corresponding to the data;
5 a data receipt detection circuit for detecting receipt
6 of plural pieces of data;
7 a longest delay data detection circuit for detecting data
8 having a longest propagation delay time; and
9 a reset circuit for receiving output from said longest
10 delay data signal detection circuit and the read clock, and
11 transmitting a reset signal to the data receipt detection
12 circuit and a read address counter of elastic store memories.
- 1 2. The elastic store circuit according to claim 1, wherein
2 said reset signal is transmitted to said data receipt
3 detection circuit through the read address counter of the
4 elastic store memories.
- 1 3. The elastic store circuit according to claim 1, wherein
2 said data receipt detection circuit comprises a plurality
3 of flip-flop circuits for receiving a frame pulse.
- 1 4. The elastic store circuit according to claim 3, wherein
2 said flip-flop circuit is a set/reset flip-flop circuit,
3 and a set terminal of the flip-flop circuit receives the frame

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4 pulse, and a reset terminal of the flip-flop circuit receives
5 the reset signal.

1 5. The elastic store circuit according to claim 1, wherein
2 said longest delay data detection circuit is an AND circuit
3 for receiving a plurality of output signals of said data receipt
4 detection circuit.

1 6. The elastic store circuit according to claim 1, wherein
2 said reset circuit comprises:
3 a flip-flop circuit for receiving the read clock; and
4 an AND circuit for outputting a reset signal upon receipt
5 of a signal from the flip-flop circuit.

1 7. An elastic store circuit which absorbs a propagation delay
2 time difference among plural pieces of data, comprising:
3 a clock selector for selecting a read clock from a
4 plurality of clocks corresponding to the data;
5 a data receipt detection circuit comprising a plurality
6 of flip-flop circuits for receiving a frame pulse;
7 a longest delay data detection circuit comprising an AND
8 circuit for receiving each output signal of said flip-flop
9 circuits;

10 a flip-flop circuit for receiving output of said longest
11 delay data detection circuit and the read clock; and
12 a reset circuit comprising a read address counter of
13 elastic store memory, and a two-input AND circuit for

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14 transmitting a reset signal to said data receipt detection
15 circuit.

1 8. A data receiving method, comprising the steps of:
2 receiving data through a plurality of transmission lines,
3 and storing the data in corresponding elastic store memory;
4 receiving a plurality of clocks and frame pulses
5 corresponding to the data;
6 selecting a read clock from the plurality of clocks;
7 receiving the frame pulses by an AND circuit, and detecting
8 receipt of a latest data; and
9 reading data from each elastic store memory according
10 to a reset signal based on output of the AND circuit and the
11 read clock.

10553602.012402